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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,225	08/19/2003	Igor Keller	CA7017522001	6463

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EXAMINER	
PIERRE LOUIS, ANDRE	
ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,225	KELLER, IGOR	
	Examiner	Art Unit	
	Andre Pierre-Louis	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 19 August 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/24/2003.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1.0 Claims 1-15 have been presented for examination.

Claim Objections

2.0 Claims 1,3,6,8,11, and 13 are objected to because of the following informalities:

2.1 Claims 1,6, and 11, refer to "the plurality of input timing events", previously there is no reference to "a plurality of input timing events". Appropriate correction is required.

2.2 Claims 3,8, and 13 refer to "selecting a worst delay further comprises", previously there is no step of "selecting a worst delay mentioned". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3.0 Claims 1-3,5-8,10-13, and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Beakes et al. (U.S. Patent No. 6,131,182).

3.1 In considering the independent claims 1,6, and 11, Beakes et al. teaches the functional equivalence of a method for determining a worst-case transition, and particularly teaches the steps of determining a plurality of output timing events for the plurality of input timing events based on a timing model of a gate *(col.13 line 24-col.14 line 42)*; and selecting a worst-case input timing event from the plurality of input timing

events based on the output timing events *(col.5 line 23-col.6 line 38; also col.8 line 58-col.9 line 34).*

3.2 As per claims 2,7, and 12, Beakes et al. teaches the step of determining a plurality of gate delays for a plurality of input signals based on the timing model of the gate *(col.14 line 9-17)*.

3.3 With regards to claims 3,8, and 13, Beakes et al. teaches the step of selecting a worst delay based on the gate delays *(col.5 line 23-col.6 line 38; also col.10 line 53-col.14 line 42).*

3.4 Regarding claims 5,10, and 15, Beakes et al. teaches that the timing model is a timing library format (FTL) model (col.8 line 58-col.10 line 12).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.0 Claims 4,9, and14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beakes et al., as applied to claims 1-3,5-8,10-13, and 15 above, in view of Jess et al. (USPG_PUB No. 2004/0002844).

4.1 Regarding claims 4,9, and 14, Beakes et al. teaches most of the instant invention; however, Beakes et al. fails to teach the timing model comprises $Dg = F(S_1, C), To = Q(^{T},,^{D}g0)$, where Dg is a gate delay, T_i is an input slew, L is a load of the gate, and To is an output slew. Jess et al. teaches the timing model comprises $Dg = F(S_1,$

C),To = Q(T,,Dg0) (pg.1 (0005-0007)), where Dg is a gate delay, T_i is an input slew, L is a load of the gate, and To is an output slew *(pg.1 (0005-0007), pg.3 (0034-0039), and pg.5-6 (0063-0069);* while Jess et al. does not include the same formula recited in the claim, the timing mode and analysis utilized by Jess et al. considers gate delay, input slew, load and output slew (*pg.1 (0005-0007), pg.3 (0034-0039), and pg.5-6 (0063-0069).* Beakes et al. and Jess et al. are analogous art because they are from the same field of endeavor and that the timing analysis used by Jess et al. is similar to the one utilized by Beakes et al. Therefore, it would have been obvious to one ordinary skilled in the art at the of the applicant's invention to combine the teachings of Beakes et al. with Jess et al. for the purpose of obtaining a more desirable timing model. Jess et al. further teaches advantage of having a more efficient system *(pg.8 (0087); see also pg.5 (0064), and pg. (0009-0014)).*

Conclusion

5.0 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5.1 Yalcin et al. (U.S. Patent No. 6,457,159) teaches a functional timing analysis for characterization of virtual component blocks.

5.2 Sheehan (USPG_PUB No. 2004/0268276) teaches an osculating models for predicting the operation of a circuit structure.

5.3 Moon et al. (U.S. Patent No. 6,928,630) teaches a timing model extraction by timing graph reduction.

5.4 Wang et al. (U.S. Patent No. 5,579,510) teaches a method and structure for use in static timing verification of synchronous circuit.

6.0 Claims 1-15 are rejected and this action is non-final. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre Pierre-Louis whose telephone number is 571-272-8636. The examiner can normally be reached on Mon-Fri, 8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 8, 2006

APL

Paul L. Rodriguez 2/10/06

Primary Examiner
Art Unit 2125